

## Product Overview

The Universal Serial Bus is a popular computer interface that has become the de-facto standard interface for PC peripherals. Now, Hi-Speed USB 2.0 is the new standard in PC peripheral connectivity. With a speed of 480Mbps, USB 2.0 is up to 40 times faster than the 12Mbps USB 1.1 most computers use today. It uses the same type cabling and is backward compatible with USB 1.1.

Implementing a USB peripheral typically requires in-depth knowledge of the USB protocol, a considerable firmware and software development effort and rigorous compliance testing. But now there's an alternative.

The QuickUSB™ QUSB2 Plug-In Module makes adding Hi-Speed USB 2.0 to new or existing products quick by integrating all the hardware, firmware and software needed to implement a general-purpose USB endpoint as an easy-to-use plug-in module. The QuickUSB™ Plug-In Module also includes the QuickUSB™ Library.

The QuickUSB plug-in module contains hardware parallel and serial ports that are connected to circuitry in the peripheral. The QuickUSB library provides user-callable software functions that transfer data to and from the hardware ports over the USB. So the designer gets multiple ports of flexible, high-speed USB connectivity and no knowledge of USB is required.

## Schematic Symbol

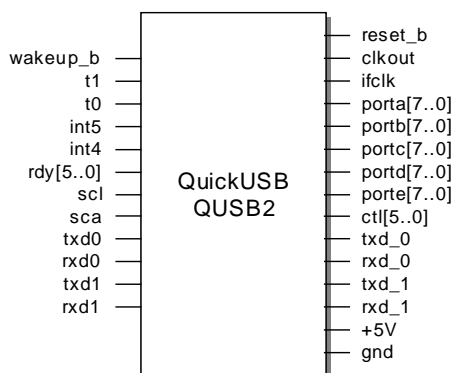


Figure 1 – QUSB2 Symbol

## Functional Description

### The QuickUSB Plug-In Module

The QuickUSB QUSB2 Plug-In Module is a 2" x 1 ½" circuit board that implements a bus-powered Hi-speed USB 2.0 endpoint terminating in a single 80-pin target interface connector.

The target interface consists of:

- One 8 or 16-bit high-speed parallel port
- Up to three general-purpose 8-bit parallel I/O ports
- Two RS-232 ports
- One I<sup>2</sup>C port
- One soft SPI port or FPGA configuration port

### High-Speed Parallel

The high-speed parallel port is configurable as an 8 or 16 bit synchronous parallel port. It delivers a sustained data rate of up to 12 MB/s and a burst rate of up to 48MB/s for packets up to 512 bytes long. The high-speed interface consists of the data port FD[15:0], control lines CMD\_DATA, REN, WEN and GPIFADR [8:0]. The port can be used as a multiplexed command/data bus by decoding CMD\_DATA (CMD = 0, DATA = 1 in the target logic. Reads are indicated by REN = 1 and writes are indicated by WEN = 1. If the address bus is configured to be active, concurrent with reads or writes the GPIFADR bus contains the address of each data element read from or written to FD [15:0].

### General Purpose Parallel I/O

General purpose I/O pins must be configured to indicate whether they are being used as input or output pins. This is accomplished using library calls documented in the QuickUSB User's Guide.

The parallel ports have multiple functions and may not be available if alternate functions are enabled. The general-purpose I/O ports are ports A, C & E. Ports B & D are reserved for the High-Speed Parallel port. The Port E alternate function is FPGA configuration and the soft SPI port. If these alternate functions are used, port E is reserved. Otherwise, port E can be used as general-purpose I/O.

### RS-232

The module has two RS-232 ports with a configurable baud rate. Both ports use the

same baud rate. These interrupt-driven ports internally buffer data as it arrives and when queried return the contents of the internal buffer. The interrupt buffer depth is 32 characters per port.

### **I<sup>2</sup>C**

An I2C compatible port is included on the QuickUSB module. The port is a bus master only. Address 1 is reserved for on-board functions. The QuickUSB library provides functions to write and read blocks of data to and from I2C peripherals.

### **SPI**

The module supports SPI peripherals through a 'soft' SPI port, which uses pins on port E. The pins MOSI, SCK, MISO and nSS are shared with the FPGA configuration function and will not interfere with each other *if* the SPI peripherals only drive the MISO when nSS is asserted (nSS=0).

### **FPGA Configuration**

The QuickUSB Plug-In Module can program SRAM-based Altera programmable logic devices using five pins of port E. When designing your peripheral to use this feature, consult the 'PS Configuration with a Microprocessor' section of Altera Application Note 116, 'Configuring SRAM-Based LUT Devices'. This document specifies the circuitry needed to configure an Altera device with a microcontroller. The QuickUSB module provides the DCLK, DATA0, nCE, nCONFIG, nSTATUS and CONF\_DONE signals required to configure Altera devices in passive-serial mode. If more than one Altera device must be configured over the interface, the devices should be 'daisy-chained' and the programming files combined into a single 'RBF' file. Consult AN116 for details on this configuration or contact Bitwise Systems.

### **The QuickUSB Library**

The QuickUSB<sup>™</sup> Library is included with the QUSB2 and provides DLL and C library interfaces to the QuickUSB Plug-in Module. The QuickUSB Library hides the complexity of USB 2.0 behind a port-based programmer's interface. A complete description of each library function is provided in the QuickUSB<sup>™</sup> User's Guide

## **Contact**

For pricing and other information contact:

Bitwise Systems  
697 Via Miguel  
Santa Barbara, CA 93111  
Phone (805) 683-6469  
Fax (805) 683-6469  
[www.bitwisesys.com](http://www.bitwisesys.com)  
[sales@bitwisesys.com](mailto:sales@bitwisesys.com)

### **UK and Europe**

#### **Contact**

**KANDA.COM**

**PO Box 200**

**Aberystwyth**

**SY23 2WD**

**UK**

**Phone/Fax : +44 (0) 8707 446 807**

**email: [sales@kanda.com](mailto:sales@kanda.com)**

**website: <http://www.kanda.com>**

## Pin Descriptions

Pin	Name	Dir	Description	Pin	Name	Dir	Description
1	GND	N/A	Ground	2	+5V	N/A	Unregulated +5V from the USB bus (300mA total)
3	PA0	I/O	Port A, Bit 0	4	RESET_B	OD	FX2 reset, Active low.
5	PA1	I/O	Port A, Bit 1	6	CLKOUT	Output	48MHz CPU clock
7	PA2	I/O	Port A, Bit 2	8	IFCLK	Output	48MHz GPIO clock
9	PA3	I/O	Port A, Bit 3	10	INT4	Input	8051 INT4 IRQ. Active high, edge sensitive
11	PA4	I/O	Port A, Bit 4	12	RXD_0	Input	Serial Port 0 RS-232 RxD
13	PA5	I/O	Port A, Bit 5	14	TXD_0	Output	Serial Port 0 RS-232 TxD
15	PA6	I/O	Port A, Bit 6	16	TXD_1	Output	Serial Port 1 RS-232 TxD
17	PA7	I/O	Port A, Bit 7	18	RXD_1	Input	Serial Port 1 RS-232 RxD
19	GND	N/A	Ground	20	+5V	N/A	Unregulated +5V from the USB bus (300mA total)
21	PB0	I/O	Port B, Bit 0 / FD0	22	CTL0	Output	GPIF ctl out 0 / CMD_DATA
23	PB1	I/O	Port B, Bit 1 / FD1	24	CTL1	Output	GPIF ctl out 1 / REN
25	PB2	I/O	Port B, Bit 2 / FD2	26	CTL2	Output	GPIF ctl out 2 / WEN
27	PB3	I/O	Port B, Bit 3 / FD3	28	CTL3	Output	GPIF ctl out 3
29	PB4	I/O	Port B, Bit 4 / FD4	30	CTL4	Output	GPIF ctl out 4
31	PB5	I/O	Port B, Bit 5 / FD5	32	CTL5	Output	GPIF ctl out 5
33	PB6	I/O	Port B, Bit 6 / FD6	34	RXD0	Input	Serial Port 0 TTL RxD (Do not use if U1 is populated)
35	PB7	I/O	Port B, Bit 7 / FD7	36	TXD0	Output	Serial Port 0 TTL TxD (Do not use if U1 is populated)
37	GND	N/A	Ground	38	+5V	N/A	Unregulated +5V from the USB bus (300mA total)
39	PC0	I/O	Port C, Bit 0 / GPIFADR0	40	RDY0	Input	GPIF input signal 0
41	PC1	I/O	Port C, Bit 1 / GPIFADR1	42	RDY1	Input	GPIF input signal 1
43	PC2	I/O	Port C, Bit 2 / GPIFADR2	44	RDY2	Input	GPIF input signal 2
45	PC3	I/O	Port C, Bit 3 / GPIFADR3	46	RDY3	Input	GPIF input signal 3
47	PC4	I/O	Port C, Bit 4 / GPIFADR4	48	RDY4	Input	GPIF input signal 4
49	PC5	I/O	Port C, Bit 5 / GPIFADR5	50	RDY5	Input	GPIF input signal 5
51	PC6	I/O	Port C, Bit 6 / GPIFADR6	52	RXD1	Input	Serial Port 1 TTL RxD (Do not use if U1 is populated)
53	PC7	I/O	Port C, Bit 7 / GPIFADR7	54	TXD1	Output	Serial Port 1 TTL TxD (Do not use if U1 is populated)
55	GND	N/A	Ground	56	+5V	N/A	Unregulated +5V from the USB bus (300mA total)
57	PD0	I/O	Port D, Bit 0 / FD8	58	PE0	I/O	Port E, Bit 0 / DATA0 / MOSI
59	PD1	I/O	Port D, Bit 1 / FD9	60	PE1	I/O	Port E, Bit 1 / DCLK / SCK
61	PD2	I/O	Port D, Bit 2 / FD10	62	PE2	I/O	Port E, Bit 2 / nCE
63	PD3	I/O	Port D, Bit 3 / FD11	64	PE3	I/O	Port E, Bit 3 / nCONFIG
65	PD4	I/O	Port D, Bit 4 / FD12	66	PE4	I/O	Port E, Bit 4 / nSTATUS
67	PD5	I/O	Port D, Bit 5 / FD13	68	PE5	I/O	Port E, Bit 5 / CONF_DONE / MISO (see note)
69	PD6	I/O	Port D, Bit 6 / FD14	70	PE6	I/O	Port E, Bit 6 / nSS
71	PD7	I/O	Port D, Bit 7 / FD15	72	PE7	I/O	Port E, Bit 7 / GPIFADR8
73	SCL	OD	Clock for I2C interface	74	WAKEUP_B	Input	USB Wakeup. Active low.
75	SDA	OD	Data for I2C interface	76	INT5_B	Input	INT5 Interrupt Request. Active low, edge sensitive
77	T0	Input	Input for Timer0	78	T1	Input	Input for Timer1
79	GND	N/A	Ground	80	+5V	N/A	+5V

Table 1 – QUSB2 Pin Description

**QuickUSB Socket Layout**

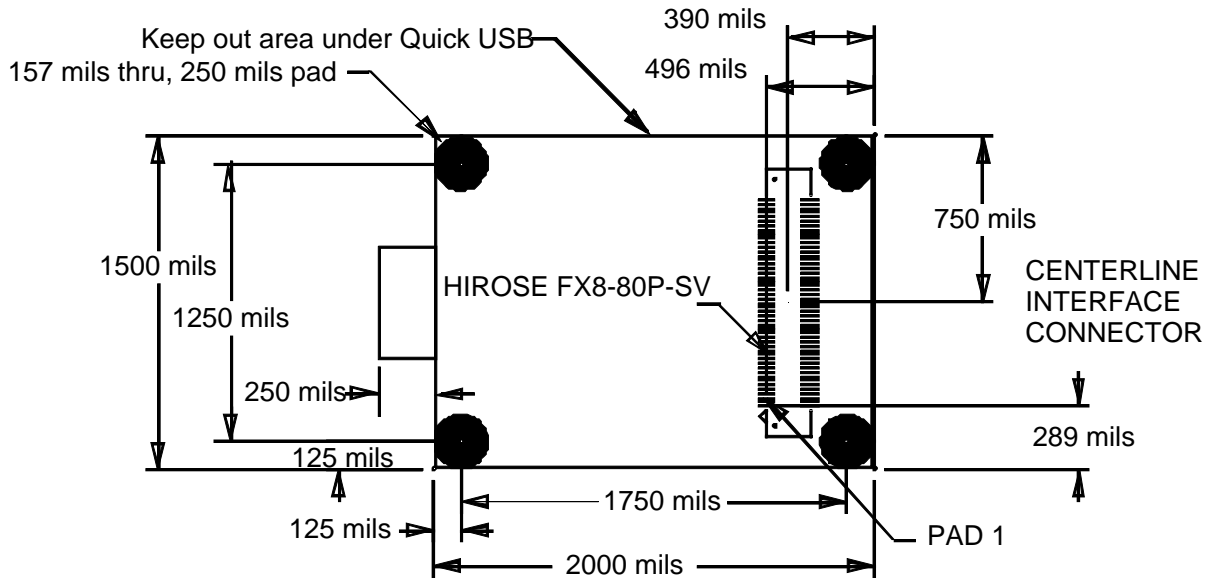


Figure 2- QuickUSB Socket Layout

**KANDA.COM**

UK and European Supplier  
PO Box 200  
Aberystwyth  
SY23 2WD  
UK  
Phone and Fax: +44 (0) 8707 446 807  
email: sales@kanda.com  
Website: <http://www.kanda.com>