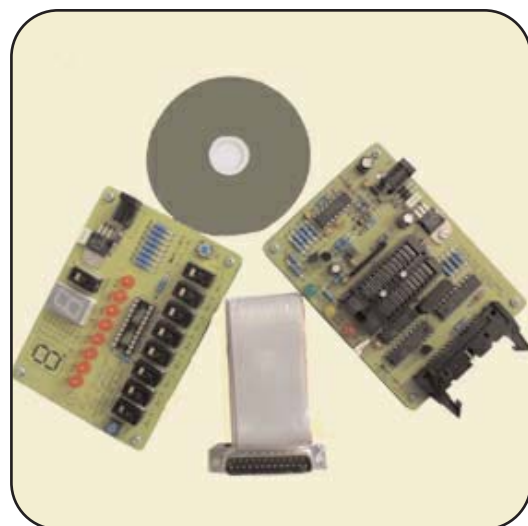


- Ideal for training
- Widely used in colleges
- For all Windows Platforms
- Also good for development
- Book on CD

# PLD Starter Kit

**A complete Starter Kit for Atmel PLD devices**



## Introduction

The PLD Starter Kit is a complete training and development package for Programmable Logic Devices.

From a training view point, the kit covers basic logic and develops the students understanding through the use of CUPL<sup>®</sup> programming language, to using PLDs in a practical design by following the examples in the book included on the CD.

For developers who do not currently use PLDs in their designs, this kit provides a platform for incorporating them. PLDs have many advantages over conventional logic chips including:

- Security - it is much harder to reverse engineer circuits using PLDs
- Space - a single PLD can replace a group of standard logic chips
- Flexible - gates can be mixed and matched rather than having to design using standard packages
- Custom - design your own custom hardware - flip-flops, latches, sequential or combinational logic circuits

## Software

The software is a complete development environment including template generator, CUPL<sup>®</sup> Compiler, editor and programming software in a single package.

### Template generator

A chip map that simplifies pin assignments and naming conventions. It ensures that I/O is correctly assigned and all the information required to generate a JEDEC output file is included

### Contents:

- Target board
- Board Schematics
- PLD device sample
- Programmer
- Complete Book on CD
- IDE with editor
- and CUPL
- Code examples
- Datasheets

### Compatible with:

- Win/95/98/ME
- Win 2000/NT4/XP

### Order Code:

**ATM014**



## Device Support

Only Atmel Flash PLDs are supported. These devices are re-programmable thousands of times.

- ATF16V8B
- AT16V8BQL
- ATF16V8C
- ATF20V8B
- ATF22V10C

This programmer does not support AT22V10B devices as these are officially obsolete

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The second part of the template generator allows pins to be named and assigned to Input or Output.

The generator then creates the PLD file in an editor window with all the necessary information. You just need to write the logic equations.

## CUPL Compiler

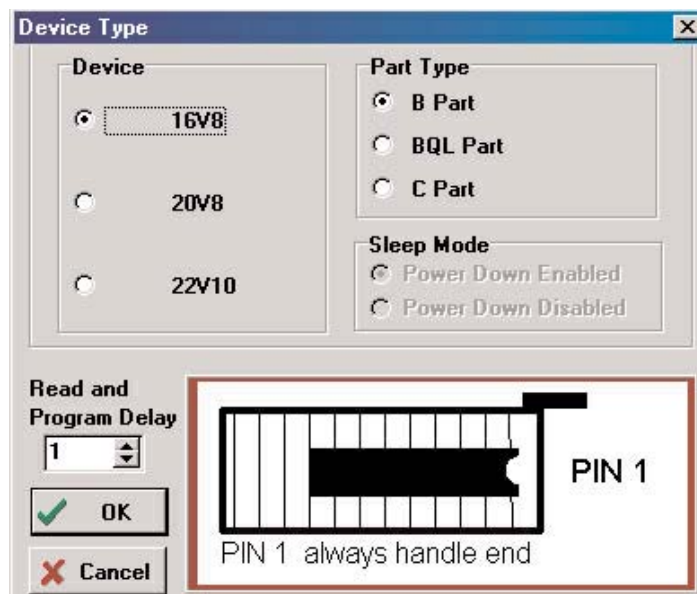
CUPL compiles the completed PLD file into a JEDEC output file. This screen allows you to set different compile options and security levels.

Errors are displayed in a separate window and detailed in the listing file. A separate manual is included for CUPL including error code descriptions.

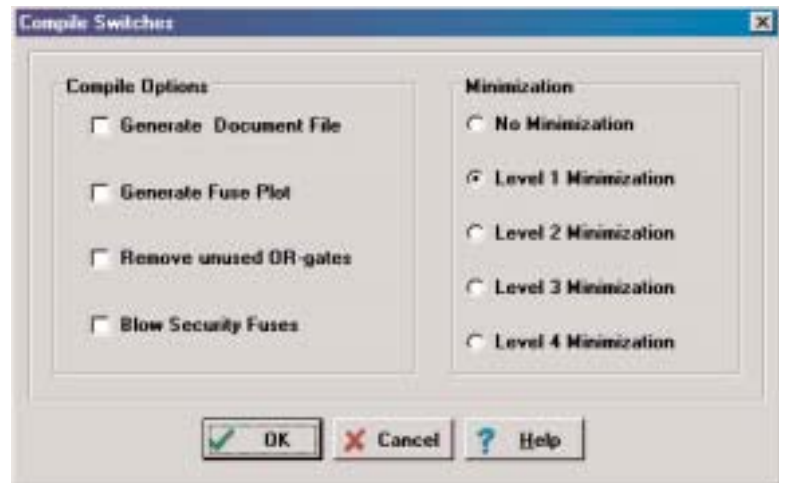
## Editor

The editor can handle multiple files and has find, copy and paste and Go to Line functions. Fonts can also be changed.

## Programmer screen



device also have Sleep Modes to reduce power consumption and this is set on the programming screen. Note that the Security bits are set during Compile and not by the programmer i.e. the security bit settings are included in JEDEC file



Once the PLD file has been compiled successfully, you can program your device using the JEDEC (.JED) file. Just set your device type in the programmer screen and the device is programmed and verified in one operation.

## Copying devices

The Read function will read the device and create a JEDEC file. This file can be saved or used to program other devices.

## Other functions

Devices can be erased using the separate Erase function. Some

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## Windows support

- Win95
- Win98
- Win NT
- Win 2000
- Win ME
- Win XP

**Order Code:**

**ATM014**

## The Book

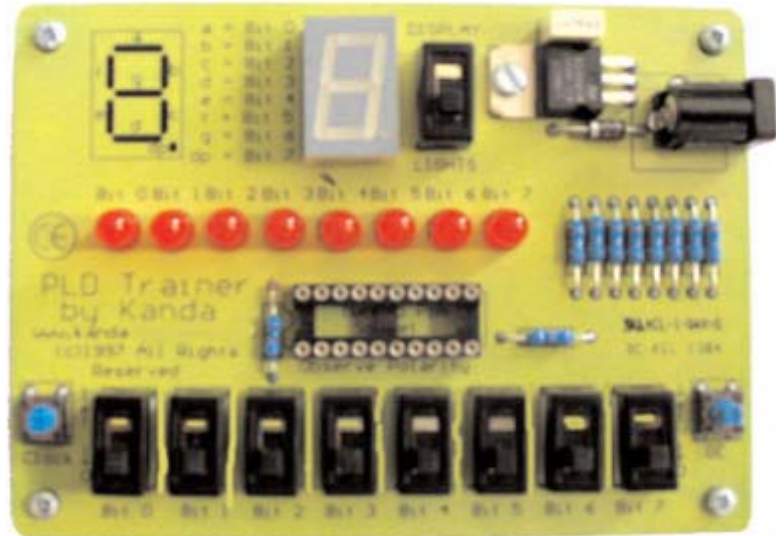
A complete book is included on the CD. It is a comprehensive guide to using PLDs with worked examples. Topics covered include

- Logic refresher: covers basic logic, minimization, latches, flipflops, BCD etc.
- Benefits of using PLDs: what are PLDs, other logic devices, industry standards
- PLD Design cycle: constructing gates, D-type flip-flops, registered designs
- Combinational design example: 7-segment display decoder
- Sequential design example: Decade up/down counter
- Power saving with PLDs: peak currents, standby, low power devices, duty cycles
- PLD design applications: 7-segement to Hex encoder - combinational
- PLD Design Applications: Vending machine - sequential
- Component reference data

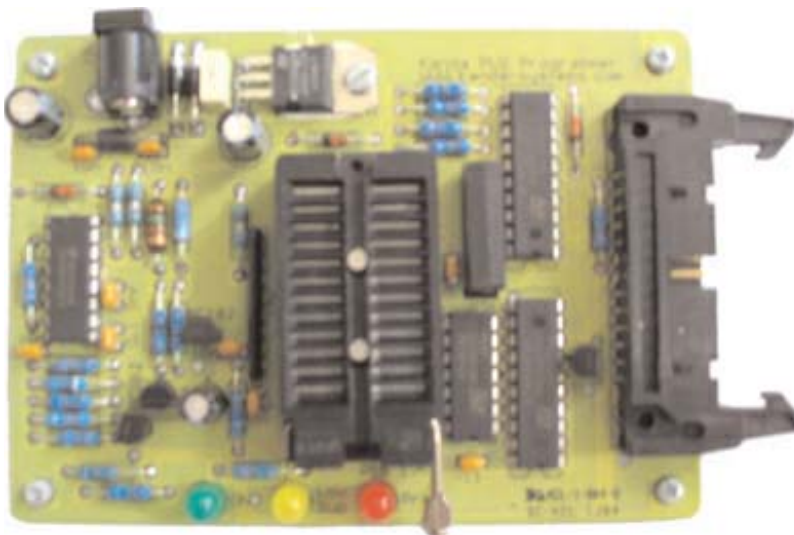
## Training Board

Included in the kit is a training board with a socket for programmed 16V8 devices. Note this board is not for use with 20V8 or 22V10 parts. Support circuitry includes 8 input switches, 8 output LEDs and a 7-segment LED display. Separate push button switches are supplied for Clock and Output Enable functions.

A schematic of the board is included on the CD



## Programming Board



The programming board features a ZIF socket for easy device insertion. It is a complete device programmer for Atmel Flash PLDs.

It has indicator lights for Power On, Input Voltage too Low and Programming in progress.

PC connection is via a 25-way parallel (Printer) port connection.

## Technical

- Power Supply requirements. The training and programming boards need 9-15VDC. Connector type is a 2.1mm barrel connector, centre positive. See PSUSTK-UK, PSU135-EU or PSU135-US for suitable PSU (wall transformers)

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- CUPL. The version of CUPL supplied with this kit is a Atmel specific DOS version which is called automatically from within all Windows operating systems. CUPL converts logic equations, pin assignments etc. included in the PLD file into a file format used by the programmer - JEDEC. JEDEC files have a standard format.

The version of CUPL supplied does not include simulation. Simulation is available in the full version of Wincupl available for free download at:

[http://www.atmel.com/dyn/products/tools\\_card.asp?tool\\_id=2759](http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2759)

You must fill in a registration card.

The full CUPL manual plus a quick start guide are included on the CD. Also available is an application note on converting ABEL files into CUPL (ABEL is the other main PLD programming language) and a CUPL Reference help file.

- 
- Physical
    - Dimensions: 200 x 120 mm (8 inches x 5 inches)
    - Package weight: 450g (16 oz)
- 

- JEDEC File format

JEDEC files must include the device type at the top, followed by security and unused fuse options.

Security:

\*F0 - no security

\*F1 - security set

Unused Fuses:

\*G0 - unblown fuses (show as 0 in Fuse Map)

\*G1 - blown fuses (show as 1 in Fuse Map)

Fuse Map:

Each line in the Fuse Map represents a 32 bit row of data. Each line starts with \*L followed by 5 address bits, then 32 bits of data. Only used lines are shown in the Fuse Map. Note JEDEC files created from reading a device will show all lines of data. The data is programmed into the device in columns not rows.

The Fuse Map of the 20V8 and 22V10 devices is shown in JEDEC format in 32 bit rows, but these devices actually have 40 fuse rows and 44 fuse rows respectively.

User data, register use, and other data is included in the last few lines of the Fuse Map

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Order Code	Description
AT16V8	Atmel ATF16V8B devices
PSU135-US	110V/13.5V Unregulated wall transformer
PSU135-EU	220V/13.5V Unregulated PSU
PSUSTK-UK	220V/15V regulated PSU



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